What is claimed is:

1. A method of fabricating a source interconnect to a memory cell, comprising:
forming a layer of dielectric material overlying a gate stack, a source region and a drain region of the memory cell;
forming a first mask layer overlying the layer of dielectric material;
patterning the first mask layer to expose a portion of the layer of dielectric material over at least the source region;
removing a portion of the exposed portion of the layer of dielectric material to expose the source region;
removing the first mask layer;
forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region;
forming a second mask layer overlying the layer of polysilicon;
patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region;
implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon;
removing the second mask layer; and
selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect.

2. The method of claim 1, wherein forming a first and/or second mask layer further comprises forming a first and/or second mask layer with a photoresist.

3. The method of claim 1, wherein patterning the first and/or second mask layer further comprises patterning the first and/or second mask layer with the same pattern.

4. The method of claim 1, wherein forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region further comprises

forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region, wherein the layer of polysilicon is conductively doped.

5. The method of claim 1, wherein selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect further comprises selectively wet etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect.

6. The method of claim 5, wherein wet etching further comprises wet etching with TMAH.

7. The method of claim 1, wherein selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect further comprises selectively wet etching the layer of polysilicon to preferentially remove the implanted portion, thereby forming the source interconnect.

8. The method of claim 7, wherein wet etching further comprises wet etching with KOH.

9. The method of claim 1, wherein forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region further comprises forming a layer of silicon-containing material overlying the layer of dielectric material and in contact with the exposed source region.

10. The method of claim 1, wherein patterning first mask layer further comprises patterning first mask layer to expose a portion of the layer of dielectric over the source region and a portion of the gate stack.

11. The method of claim 1, wherein patterning second mask layer further comprises patterning second mask layer to expose a portion of the layer of polysilicon over the source region and a portion of the gate stack.

12. The method of claim 1, wherein implanting ions further comprises implanting ions with a dosage level in the range of $1x10^{15}$ ions per cm^3 to $1x10^{22}$ ions per cm^3.

13. The method of claim 12, wherein the ion dosage level is in the range of $5x10^{18}$ ions per cm^3 to $5x10^{20}$ ions per cm^3.

14. The method of claim 1, wherein implanting ions further comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon, and silicon.

15. The method of claim 1, wherein removing the first and/or second mask layer further comprises stripping the first and/or second mask layer.

16. The method of claim 1, wherein removing a portion of the exposed portion of the layer of dielectric material to expose the source region further comprises anisotropically etching the exposed portion of the layer of dielectric material.

17. The method of claim 1, wherein patterning first and second mask layers further comprises patterning first and second mask layers to additionally expose a portion of the layer of dielectric over at least the drain region.

18. A method of fabricating a local interconnect, comprising:
forming a dielectric layer having one or more trenches formed in it;
depositing a layer of silicon-containing material over the dielectric layer;
selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches; and

wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches.

19. The method of claim 18, wherein depositing a layer of silicon-containing material further comprises depositing a layer of polysilicon.

20. The method of claim 19, wherein depositing a layer of polysilicon further comprises depositing a layer of conductively doped polysilicon.

21. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches and wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material that is not over the one or more trenches and wet etching the layer of silicon-containing material to remove the implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches.

22. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches and wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches and wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches, where the one or more formed silicon-containing material local interconnect lines have a "T" or "Y" shaped cross section.

23. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches and wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches and wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches, where a top portion of the one or more formed silicon-containing material local interconnect lines overlap portions of one or more structural features surrounding of the trench or contact hole.

24. The method of claim 18, wherein forming a dielectric layer having one or more trenches formed in it and depositing a layer of silicon-containing material over the dielectric layer further comprises forming a dielectric layer having one or more trenches formed in it and depositing a layer of silicon-containing material over the dielectric layer, where one or more contact holes are formed in the one or more trenches and the silicon-containing material is coupled to one or more source regions through the one or more contact holes formed in the one or more trenches.

25. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material to an implant depth that is one half of a thickness of the layer of silicon-containing material.

26. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material with a dosage level in the range of $1x10^{15}/cm^3$ to $1x10^{22}/cm^3$.

27. The method of claim 26, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material with a dosage level in the range of $1x10^{15}/cm^3$ to $1x10^{22}/cm^3$ further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material with a dosage level in the range of $5x10^{18}/cm^3$ to $5x10^{20}/cm^3$.

28. The method of claim 18, wherein selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of silicon-containing material with an ion species that is one of boron, arsenic, phosphorus, argon, and silicon.

29. The method of claim 18, depositing a layer of silicon-containing material over the dielectric layer further comprises depositing a layer of silicon-containing material over the dielectric layer, where the layer of silicon-containing material has a thickness such that the layer of silicon-containing material will pinch off when filling the one or more trenches and/or contact holes.

30. The method of claim 18, wherein wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches further comprises wet etching the layer of silicon-containing material with one of an acid solution and a base solution, wherein the acid and/or base solution is selective over ion implanted and non-ion implanted silicon-containing material.

31. The method of claim 18, wherein wet etching the layer of silicon-containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect lines in the one or more trenches further comprises wet etching the layer of silicon-containing material with one of TMAH and KOH.

32. A method of fabricating a memory array, comprising:

forming a plurality of word line gate stacks, each containing a plurality of memory cells;

forming a dielectric layer having one or more trenches;

depositing a layer of polysilicon over the dielectric layer;

selectively implanting ions in one or more regions of the layer of polysilicon over the trenches; and

wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches.

33. The method of claim 32, wherein forming a dielectric layer having one or more trenches further comprises forming a dielectric layer having one or more trenches, where the trenches are formed over one or more source regions of the word line gate stacks.

34. The method of claim 32, wherein the memory array is one of a Flash memory array and a EEPROM memory array.

35. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches, where the one or more formed polysilicon local interconnect lines are coupled to one or more source regions.

36. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to

remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon over one or more drain regions and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more bit line contacts, where the one or more formed bit line contacts are coupled to the one or more drain regions.

37. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches, where a top portion of the one or more formed polysilicon local interconnect lines overlap portions of one or more structural features surrounding of the trench or contact hole.

38. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon to an implant depth that is one half of a thickness of the layer of polysilicon.

39. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon with a dosage level in the range of $1x10^{15}/cm^3$ to $1x10^{22}/cm^3$.

40. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches further comprises selectively implanting ions

in one or more regions of the layer of polysilicon with an ion species that is one of boron, arsenic, phosphorus, argon, and silicon.

41. The method of claim 32, depositing a layer of polysilicon over the dielectric layer further comprises depositing a layer of polysilicon over the dielectric layer, where the layer of polysilicon has a thickness such that the layer of polysilicon will pinch off when filling the one or more trenches and/or contact holes.

42. The method of claim 32, wherein wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches and/or contact holes further comprises wet etching the layer of polysilicon with one of TMAH and KOH.

43. The method of claim 32, wherein wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises wet etching the layer of polysilicon with a wet etch that is selective over one of ion implanted polysilicon and non-ion implanted polysilicon.

44. The method of claim 32, wherein selectively implanting ions in one or more regions of the layer of polysilicon over the trenches and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon that are not overlying the trenches and wet etching the layer of polysilicon to remove the implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches.

45. A method of fabricating a memory cell, comprising:
forming a memory cell having a source and a source region and a drain region; and

forming a local interconnect of polysilicon to contact to the source and/or drain region of the memory cell by the steps of,

forming a dielectric layer over the memory cell having at least one contact hole to the source/drain region of the memory cell;

depositing a layer of polysilicon overlying the dielectric layer to contact the source and/or drain region of the memory cell through the at least one contact hole of the dielectric layer,

selectively implanting ions in one or more selected regions of the layer of polysilicon, and

wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon contact from the selected regions of the layer of polysilicon.

46. The method of claim 45, wherein wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon contact from the selected regions of the layer of polysilicon further comprises wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon.

47. The method of claim 45, wherein the memory cell is a floating gate memory cell.

48. The method of claim 46, wherein selectively implanting ions in one or more selected regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon contact from the selected regions of the layer of polysilicon further comprises selectively implanting ions in one or more selected regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon, where a top portion of the at least one

formed polysilicon local interconnect line overlaps one or more structural features of the memory cell and/or one or more structural features surrounding memory cell.

49. The method of claim 45, wherein selectively implanting ions in one or more selected regions of the layer of polysilicon further comprises selectively implanting ions in one or more selected regions of the layer of polysilicon with a dosage level in the range of $1x10^{15}/cm^3$ to $1x10^{22}/cm^3$.

50. The method of claim 45, wherein selectively implanting ions in one or more selected regions of the layer of polysilicon further comprises selectively implanting ions in one or more selected regions of the layer of polysilicon with an ion species that is one of boron, arsenic, phosphorus, argon, and silicon.

51. The method of claim 45, wherein wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon contact from the selected regions of the layer of polysilicon further comprises wet etching the layer of polysilicon with a wet etch that is selective over one of ion implanted polysilicon and non-ion implanted polysilicon.

52. A method of forming a floating-gate memory cell, comprising:
forming a gate stack, comprising:
forming a tunnel dielectric layer overlying a semiconductor substrate;
forming a floating-gate layer overlying the tunnel dielectric layer;
forming an intergate dielectric layer overlying the floating-gate layer; and
forming a control gate layer overlying the intergate dielectric layer;
forming a drain region in the substrate on a first side of the gate stack;
forming a source region in the substrate on a second side of the gate stack;
forming a dielectric spacer layer over the gate stack having at least one contact hole to the source region of the memory cell;

depositing a layer of polysilicon overlying the dielectric spacer layer to contact the source region of the memory cell through the at least one contact hole of the dielectric spacer;

selectively implanting ions in one or more selected regions of the layer of polysilicon; and

wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon.

53. The method of claim 52, further comprising:
forming the control gate from polysilicon material; and
forming a silicide layer on the control gate layer.

54. The method of claim 52, further comprising forming a cap layer overlying the gate stack.

55. The method of claim 52, wherein the drain and source regions are formed before forming the gate stack.

56. The method of claim 52, wherein depositing a layer of polysilicon to contact at least one of the source region of the memory cell through the at least one contact hole of the dielectric spacer further comprises depositing a layer of conductively doped polysilicon.

57. The method of claim 52, wherein forming a dielectric spacer layer over the gate stack having at least one contact hole to the source region of the memory cell and depositing a layer of polysilicon overlying the dielectric spacer layer to contact the source region of the memory cell through the at least one contact hole of the dielectric spacer further comprises forming a dielectric spacer layer over the gate stack having at least one contact hole to the drain region of the memory cell depositing a layer of polysilicon

overlying the dielectric spacer layer to contact the drain region of the memory cell through the at least one contact hole of the dielectric spacer.

58. The method of claim 52, wherein wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon further comprises wet etching the layer of polysilicon to remove the implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the non-selected regions of the layer of polysilicon.

59. The method of claim 52, wherein selectively implanting ions in one or more selected regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon further comprises selectively implanting ions in one or more selected regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon, where a top portion of the at least one formed polysilicon local interconnect line overlaps the dielectric spacer and gate stack and/or one or more structural features surrounding memory cell.

60. A method of forming an array of floating-gate memory cells, comprising:
forming a first dielectric layer on a silicon substrate;
forming a first polysilicon layer on the first dielectric layer;
forming a second dielectric layer on the first polysilicon layer;
forming a second polysilicon layer on the second dielectric layer;
forming a third dielectric layer overlying the second polysilicon layer;
patterning the first dielectric layer, the first polysilicon layer, the second dielectric layer, the second polysilicon layer, and the third dielectric layer to define word line gate stacks;
forming source and drain regions between adjacent word line gate stacks;

forming dielectric spacer layer over the word line gate stacks;

removing a portion of the dielectric spacer layer to define trenches exposing source regions, wherein each trench exposes a plurality of source regions;

depositing a third polysilicon layer over the dielectric spacer layer, where the third polysilicon layer fills the trenches;

selectively implanting ions in one or more regions of the third polysilicon layer; and

wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches.

61. The method of claim 60, wherein selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches, where a top portion of the one or more formed polysilicon local interconnect line overlap a portion of the word line gate stacks.

62. The method of claim 60, further comprising;

removing a portion of the dielectric spacer layer to define one or more contact holes exposing drain regions, wherein each contact hole exposes one drain region;

selectively implanting ions in one or more regions of the third polysilicon layer; and

wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon drain contacts in the one or more contact holes.

63. The method of claim 60, wherein forming the source and drain regions occurs prior to patterning the layers.

64. The method of claim 60, wherein removing a portion of the insulator layer to define trenches exposing source regions further comprises exposing source regions along an entire length of a word line gate stack.

65. The method of claim 60, further comprising:

forming a bit line coupled to drain regions of a column of memory cells, wherein the bit line is individually coupled to each drain region of the column of memory cells;

forming at least one contact to a word line gate stack of a row of memory cells; and

forming at least one contact to source regions of the row of memory cells.

66. The method of claim 60, wherein selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches.

67. The method of claim 60, wherein selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the third polysilicon layer and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysilicon source local interconnect lines in the one or more trenches.

68. A method of forming a floating gate memory, comprising:

forming a plurality of word line gate stacks, each containing a plurality of floating gate memory cells;

forming a spacer dielectric layer overlying the plurality of word line gate stacks having one or more trenches, where the one or more trenches expose one or more source regions of the plurality of memory cells;

depositing a layer of polysilicon overlying the spacer dielectric layer;

selectively implanting ions in one or more regions of the layer of polysilicon; and

wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches.

69. The method of claim 68, wherein the memory is one of a Flash memory and an EEPROM memory.

70. The method of claim 68, wherein selectively implanting ions in one or more regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches.

71. The method of claim 68, wherein selectively implanting ions in one or more regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches further comprises selectively implanting ions in one or more regions of the layer of polysilicon and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches, where a top portion of the one or more formed polysilicon local interconnect lines overlap portions of the adjacent word line gate stacks.

72. A floating-gate memory cell, comprising:

a tunnel dielectric layer formed overlying a semiconductor substrate;

a drain region formed in a semiconductor substrate adjacent a first side of the tunnel dielectric layer;

a source region formed in a semiconductor substrate adjacent a second side of the tunnel dielectric layer;

a floating-gate layer formed overlying the tunnel dielectric layer;

an intergate dielectric layer formed overlying the floating-gate layer;

a control-gate layer formed overlying the intergate dielectric layer;

a first contact coupled to the source region; and

wherein the first contact comprises a polysilicon layer with an ion implanted top layer.

73. The floating-gate memory cell of claim 72, further comprising:

a second contact to the drain region, wherein the second contact comprises a polysilicon layer with an ion implanted top layer.

74. The floating-gate memory cell of claim 72, wherein the control-gate layer comprises a silicide layer in contact with an underlying polysilicon layer.

75. The floating-gate memory cell of claim 72, further comprising:

a word line cap dielectric layer formed overlying the control-gate layer.

76. The floating-gate memory cell of claim 72, wherein there is no interposing dielectric layer between the control-gate layer and an overlying bulk insulator layer.

77. The floating-gate memory cell of claim 72, wherein the polysilicon layer of the first contact has a "T" or "Y" shaped cross sectional area.

78. The floating-gate memory cell of claim 72, wherein the polysilicon layer of the first contact is in contact with a source region of one or more other floating-gate memory cells.

79. A memory device, comprising:

an array of floating-gate memory cells, wherein the array comprises:

a plurality of rows of memory cells, each row coupled to a word line;

a plurality of columns of memory cells, each column coupled to a bit line;

a plurality of array source interconnects, each interconnect coupled to source regions of at least a portion of a row of memory cells; and

a plurality of drain contacts, each drain contact coupled between a drain region of a memory cell and a bit line; and

wherein each array source interconnect comprises a polysilicon layer with an ion implanted top layer, where each array source interconnect is in contact with its associated source regions.

80. The memory device of claim 79, wherein the memory device is one of a Flash memory device and a EEPROM memory device.

81. The memory device of claim 79, wherein each drain contact further comprises a polysilicon layer with an ion implanted top layer, where each drain contact is coupled to its associated drain region.

82. The memory device of claim 79, further comprising:

a word line cap dielectric layer formed overlying the control-gate layer.

83. The memory device of claim 79, wherein the polysilicon layer of each array source interconnect overlays the adjacent memory cell rows.

84. The memory device of claim 79, wherein the polysilicon layer of each array source interconnect has a "T" or "Y" shaped cross sectional area.

85. The memory device of claim 79, wherein the at least one array source interconnect is coupled to source regions of an entire row of memory cells.

86. A system, comprising:

a processor coupled to a memory device, wherein the memory device comprises,

an array of floating-gate memory cells, wherein the array comprises:

a plurality of rows of memory cells, each row coupled to a word line;

a plurality of columns of memory cells, each column coupled to a bit line;

a plurality of array source interconnects, each interconnect coupled to source regions of at least a portion of a row of memory cells; and

a plurality of drain contacts, each drain contact coupled between a drain region of a memory cell and a bit line; and

wherein each array source interconnect comprises a polysilicon layer with an ion implanted top layer, where each array source interconnect is coupled to its associated source regions.

87. The system of claim 86, wherein the memory array is one of a Flash memory array and an EEPROM memory array.